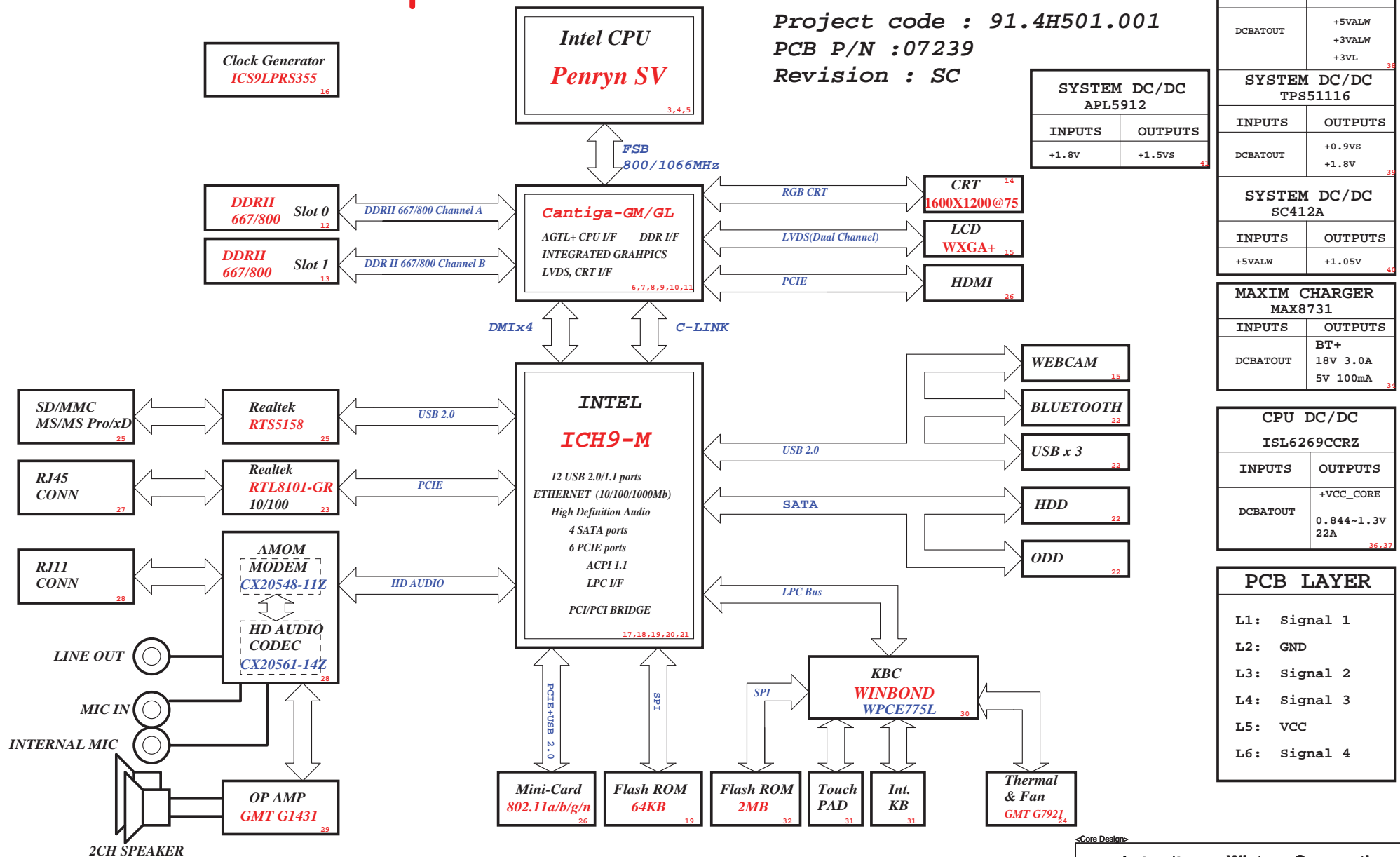


Warrior Intel UM Block Diagram

<http://hobi-elektronika.net>



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Page 12

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9 Integrated pull-up and pull-down Resistors

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SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

Page 19

LANE1	LAN
LANE2	MiniCard WLAN

USB Table

Page 19

Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus

KBC

ICH9M

Thermal

BATTERY

MINI

Clock Generator

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Wistron Corporation

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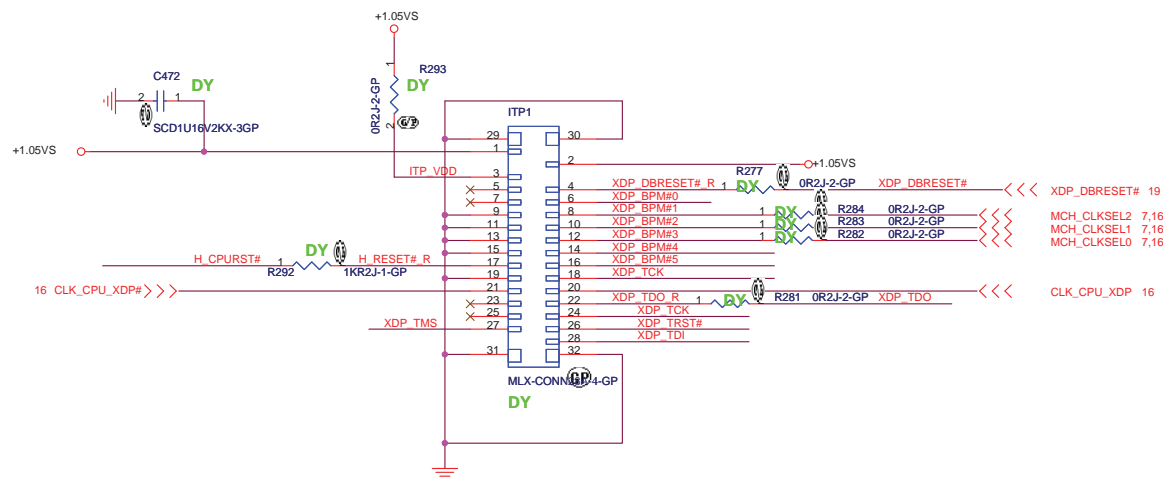
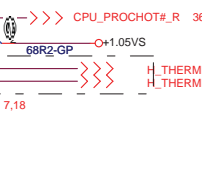
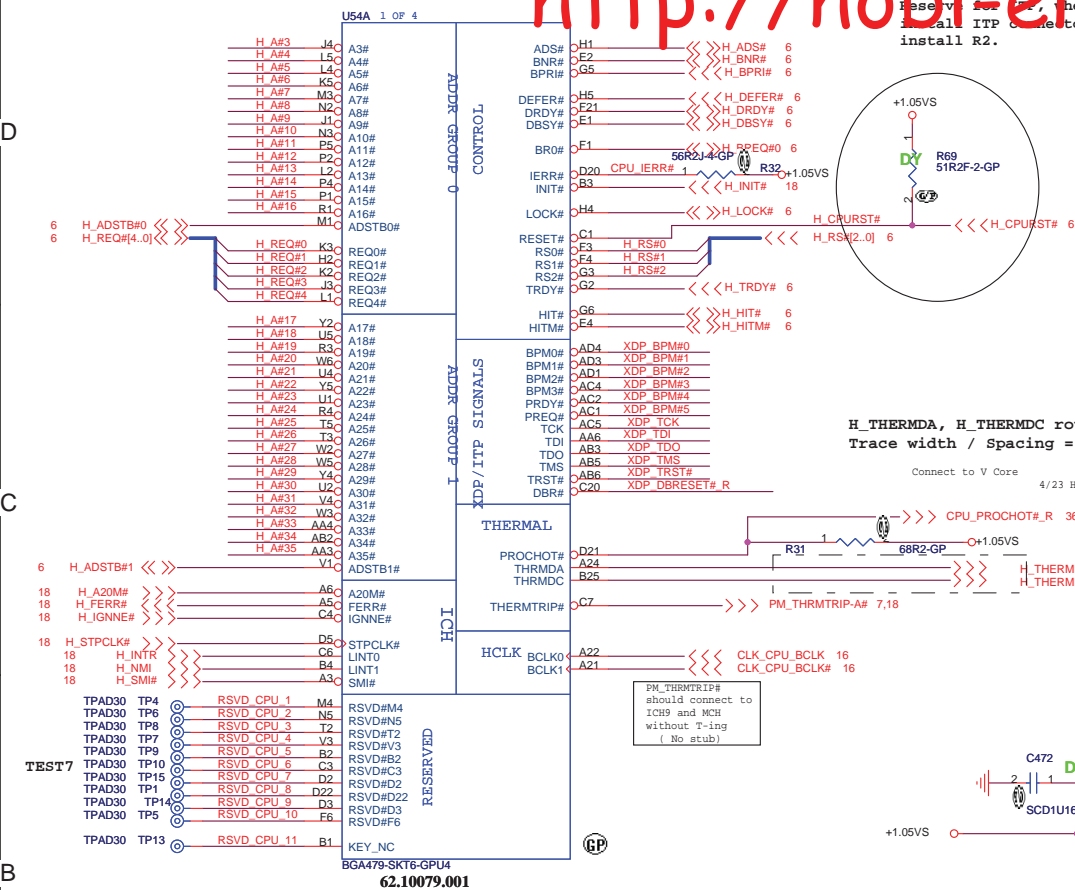
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SC

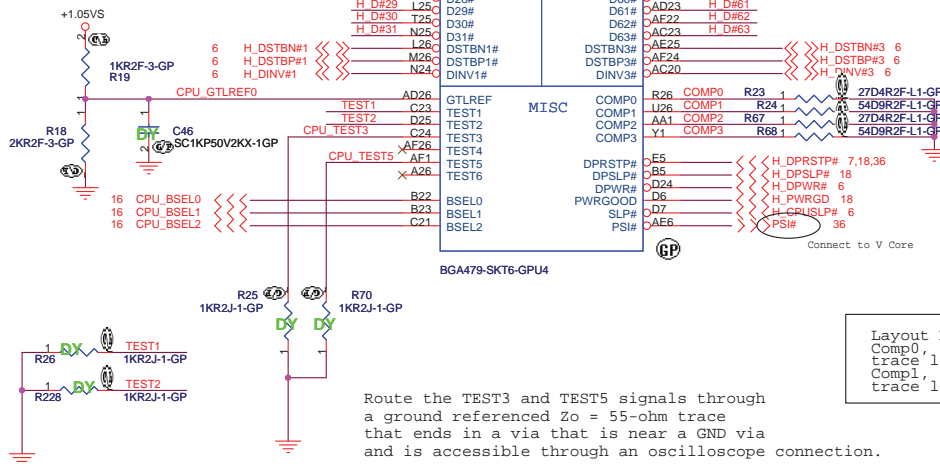
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Sheet 2 of 42



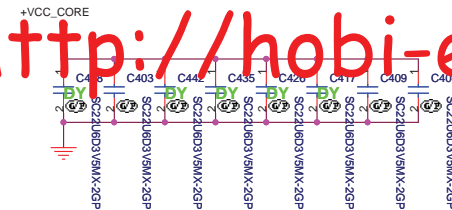
<Core Design> Place R310 with in 200ps (~1") to CPU

Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF

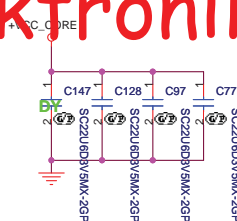


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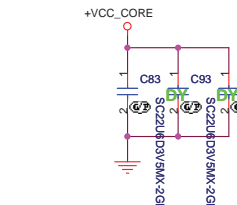
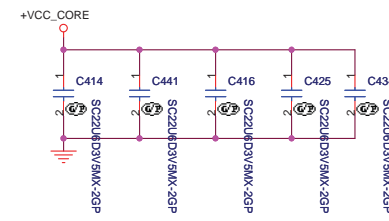
Please these inside socket cavity on L8(North side Secondary)



Please these outside socket cavity on L8(North side Secondary)

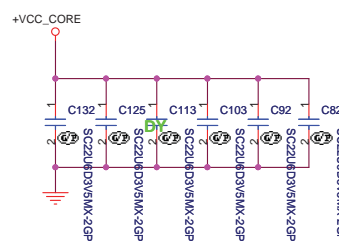
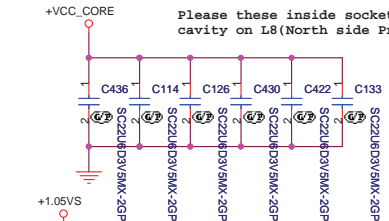


Please these inside socket cavity on L8(South side Secondary)

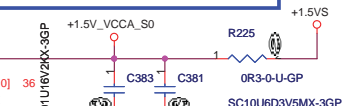


Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)



layout note: "1b5V_VCCA_S0" as short as possible

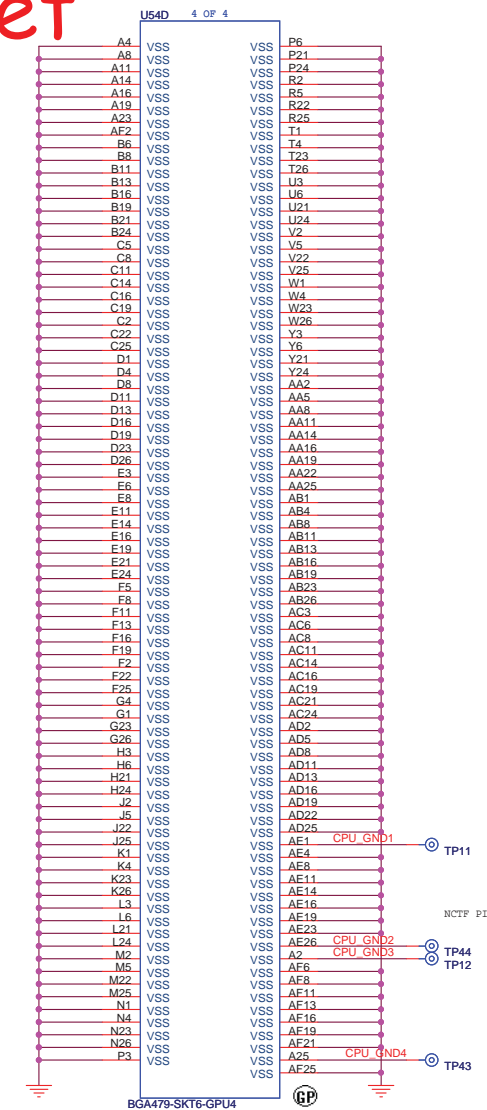
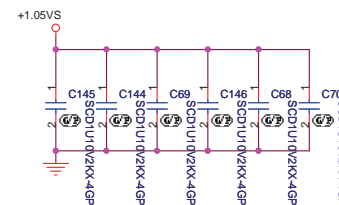


Layout Note: Place as close as possible to the CPU VCCA pin.

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

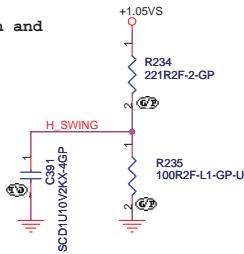
Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)

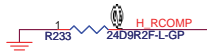


H_SWING routing Trace width and Spacing use 10 / 20 mil

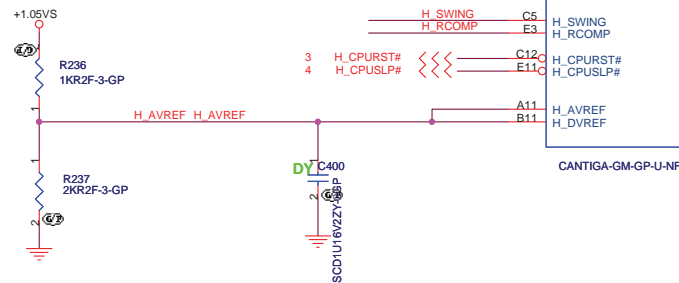
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



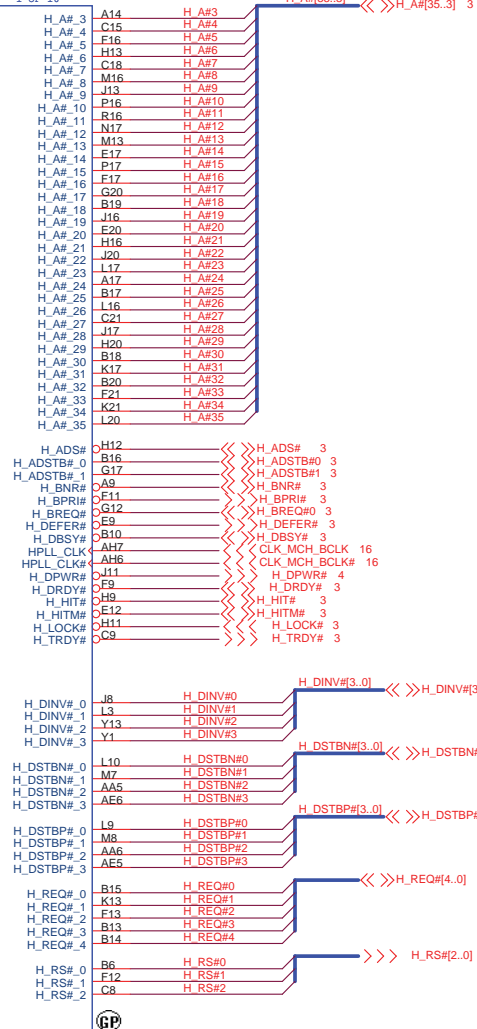
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



ISOH



<Core Design>

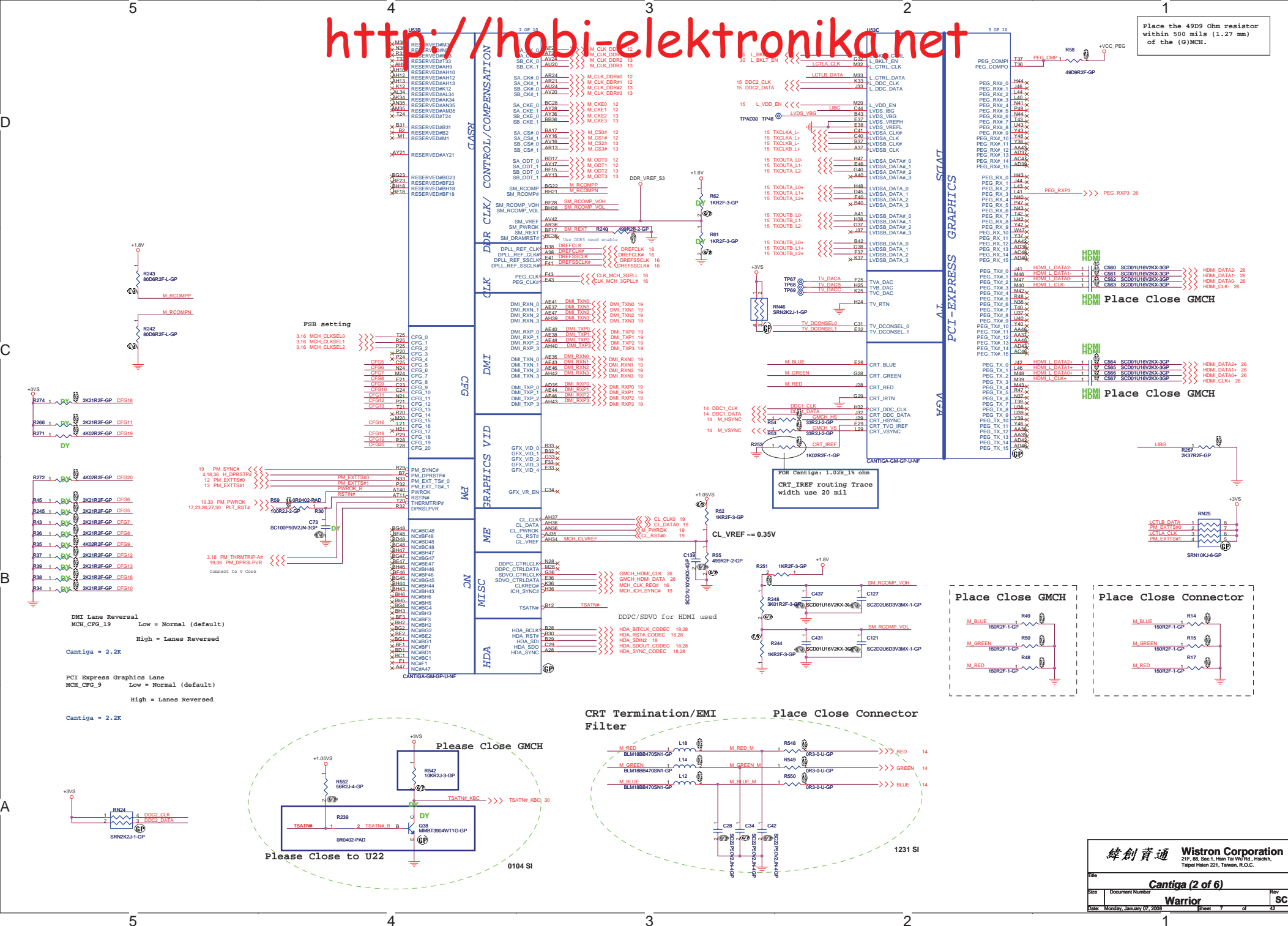
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Taipei Hsien 221, Taiwan, R.O.C.

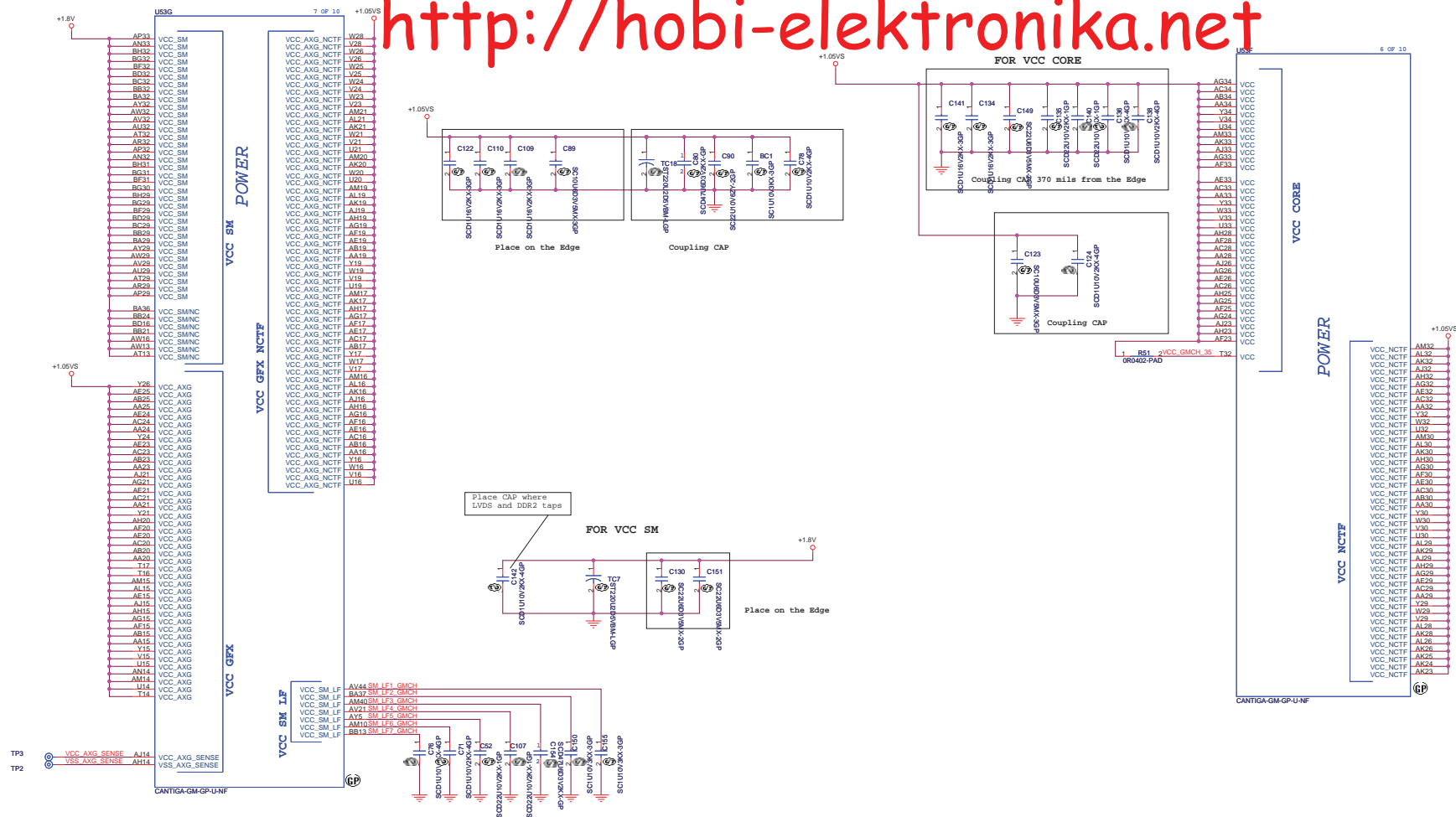
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Rev SC

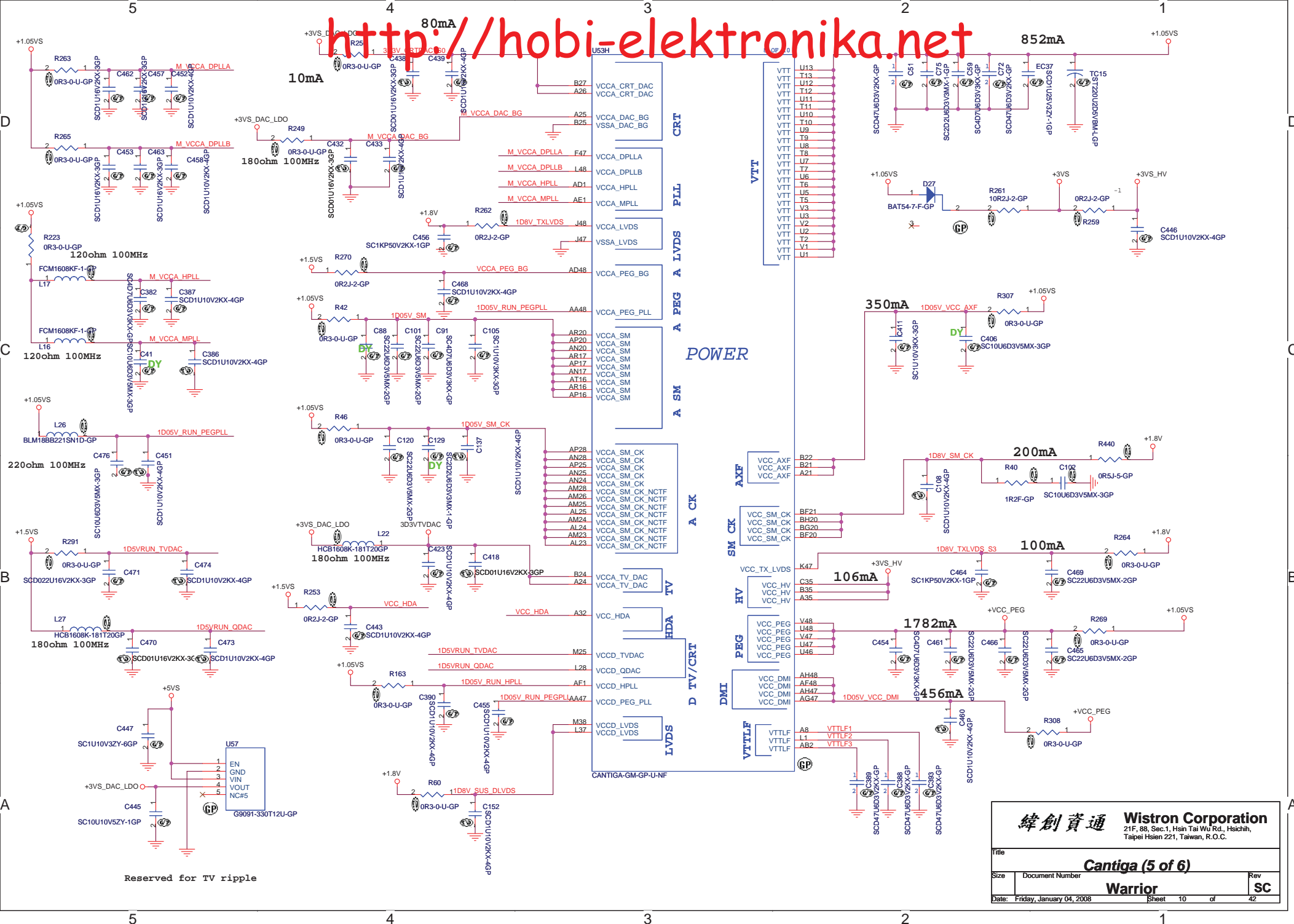
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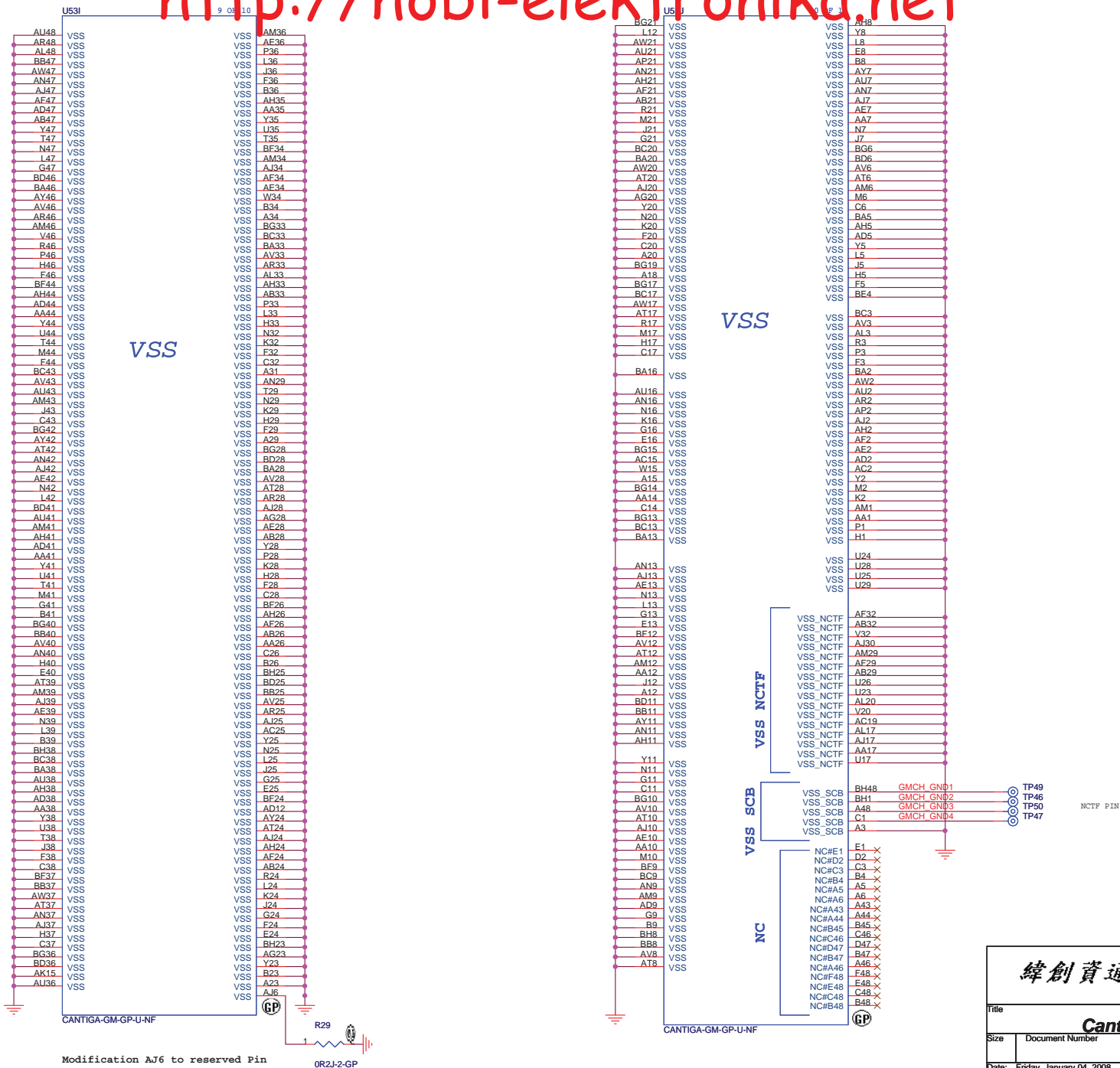
Warrior

Place the 49D9 Ohm resistor
within 500 mils (1.27 mm)
of the (G)MCH.



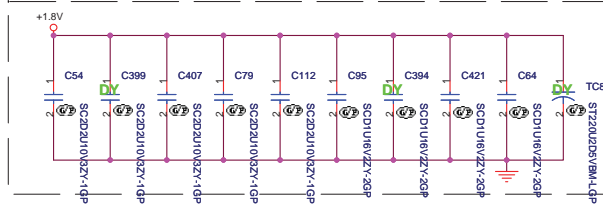




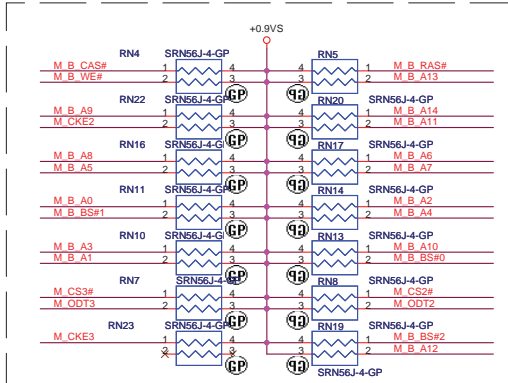
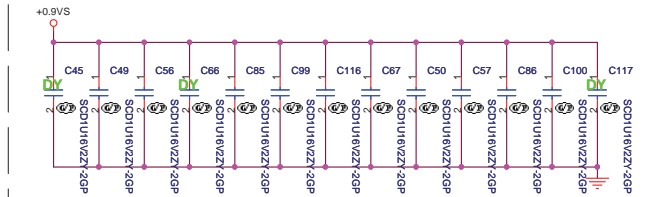


8 M_B_DQS#(7..0) <<>
 8 M_B_DQ(63..0) <<>
 8 M_B_DM(7..0) <<>
 8 M_B_DQS(7..0) <<>
 8 M_B_A[14..0] <<>

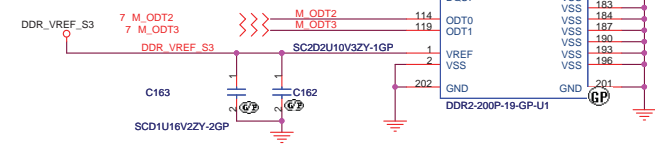
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



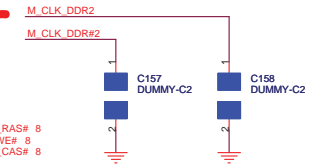
Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



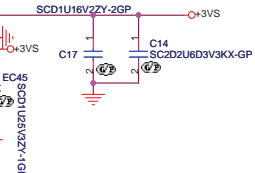
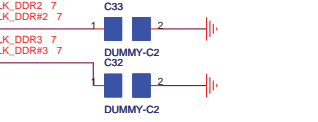
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M_B_A1	101	A1
M_B_A2	100	A2
M_B_A3	99	A3
M_B_A4	98	A4
M_B_A5	97	A5
M_B_A6	96	A6
M_B_A7	95	A7
M_B_A8	94	A8
M_B_A9	93	A9
M_B_A10	92	A10
M_B_A11	91	A11
M_B_A12	90	A12
M_B_A13	89	A13
M_B_A14	88	A14
M_B_BS#2	87	A15
M_B_BS#0	86	A16/BA2
M_B_BS#1	85	
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	17	DQ2
M_B_DQ3	19	DQ3
M_B_DQ4	6	DQ4
M_B_DQ5	23	DQ5
M_B_DQ6	14	DQ6
M_B_DQ7	16	DQ7
M_B_DQ8	25	DQ8
M_B_DQ9	28	DQ9
M_B_DQ10	35	DQ10
M_B_DQ11	37	DQ11
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M_B_DQ15	38	DQ15
M_B_DQ16	43	DQ16
M_B_DQ17	45	DQ17
M_B_DQ18	55	DQ18
M_B_DQ19	57	DQ19
M_B_DQ20	44	DQ20
M_B_DQ21	46	DQ21
M_B_DQ22	56	DQ22
M_B_DQ23	58	DQ23
M_B_DQ24	61	DQ24
M_B_DQ25	63	DQ25
M_B_DQ26	73	DQ26
M_B_DQ27	75	DQ27
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M_B_DQS#4	129	DQS4
M_B_DQS#5	146	DQS5
M_B_DQS#6	167	DQS6
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M_B_DQS3	131	DQS3
M_B_DQS4	148	DQS4
M_B_DQS5	169	DQS5
M_B_DQS6	188	DQS6
M_B_DQS7	188	DQS7
M_ODT2	114	ODT0
M_ODT3	119	ODT1
DDR_VREF_S3	1	VREF
DDR2-200P-19-GP-U1	201	GND

DM1 use 62.10017.B51

1206 SI



put near connector



<Core Design>

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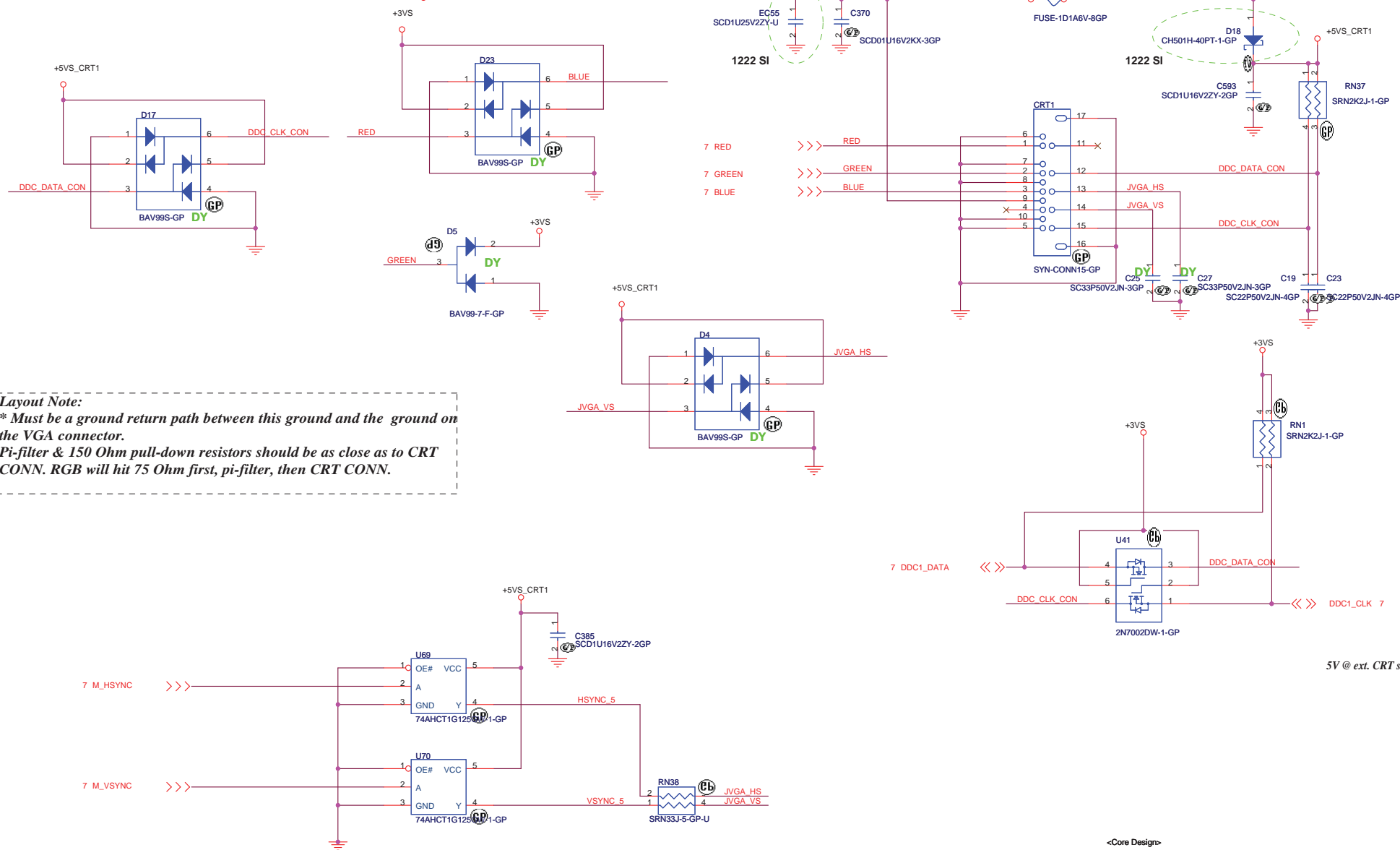
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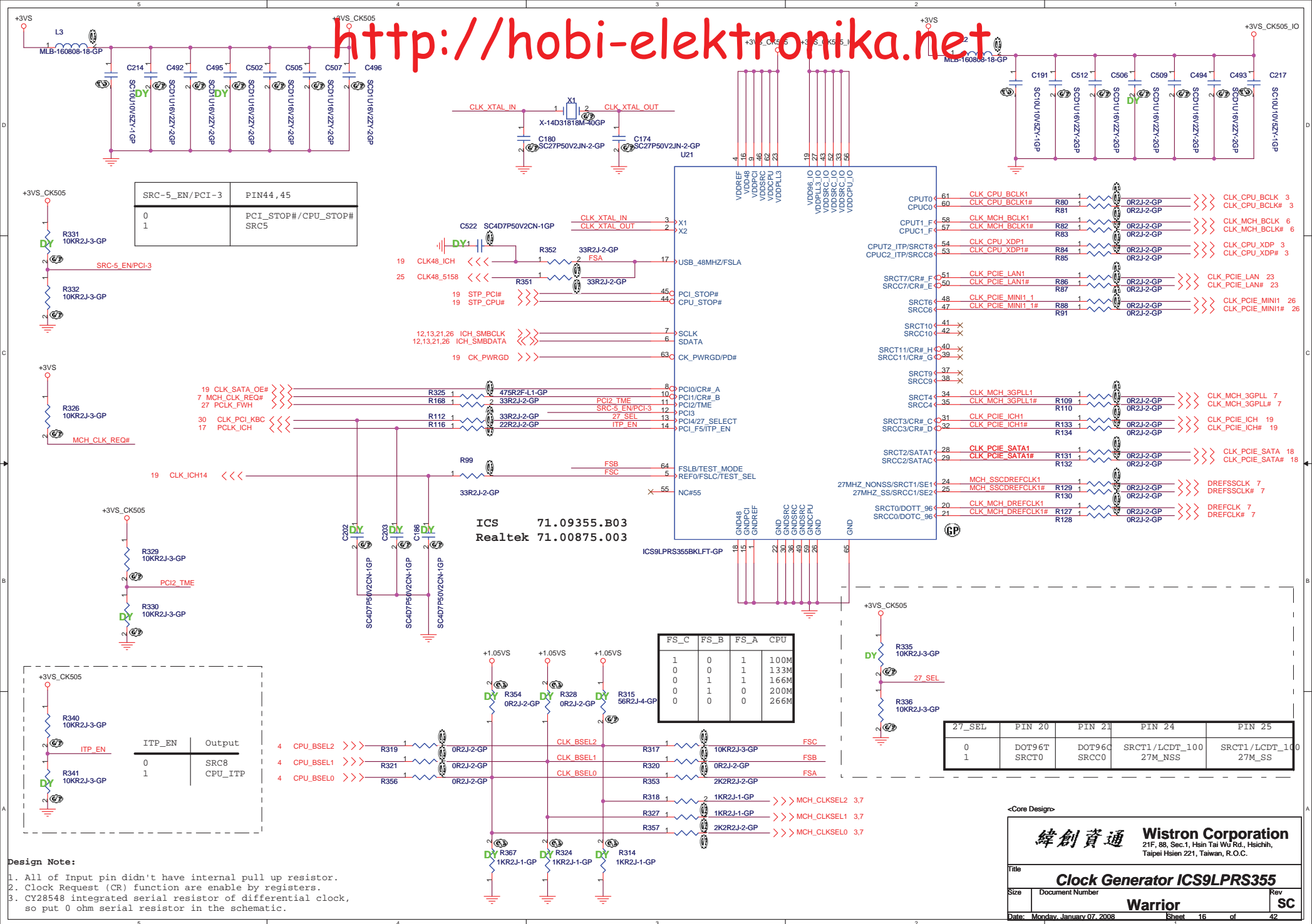
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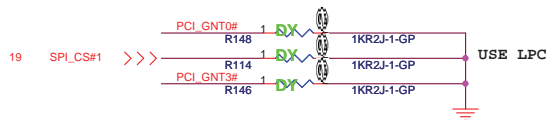
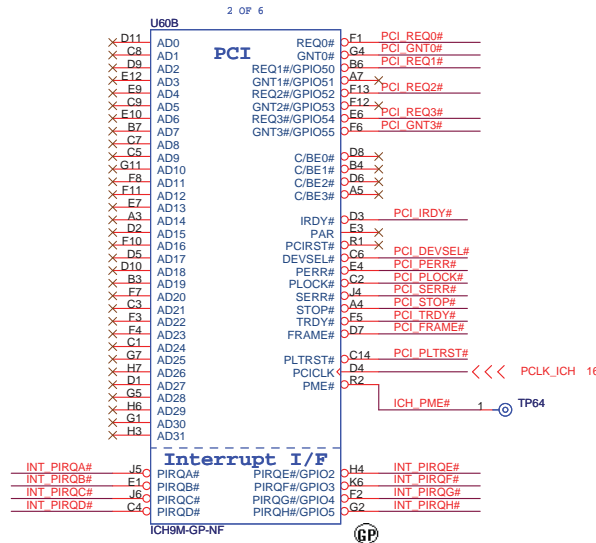
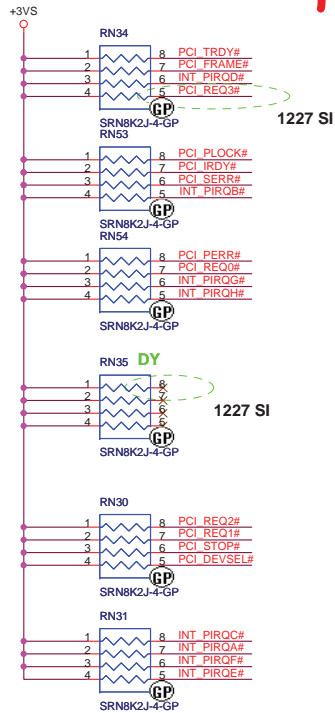




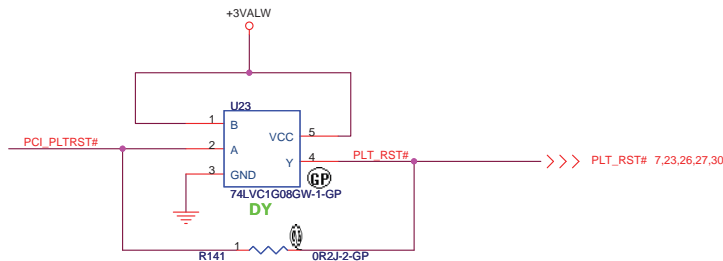
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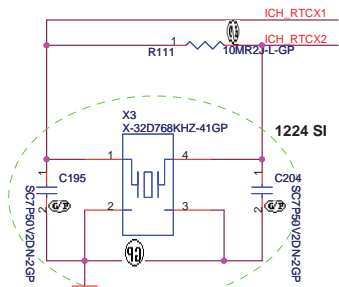
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Size	Document Number	Rev
	Warrior	SC
Date: Monday, January 07, 2008	Sheet 16 of	42



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



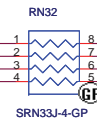
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82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm

GLAN_COMP place within 500 mil of ICH9M

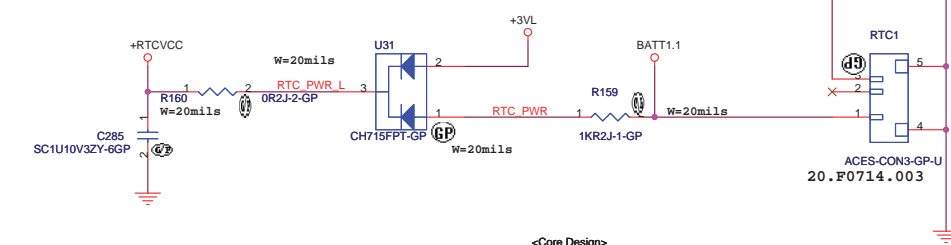
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7.28 HDA_BITCLK_CODEC
7.28 HDA_SYNC_CODEC
7.28 HDA_SDOUT_CODEC



HDD

ODD

ICH9M-GP-NF



Integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

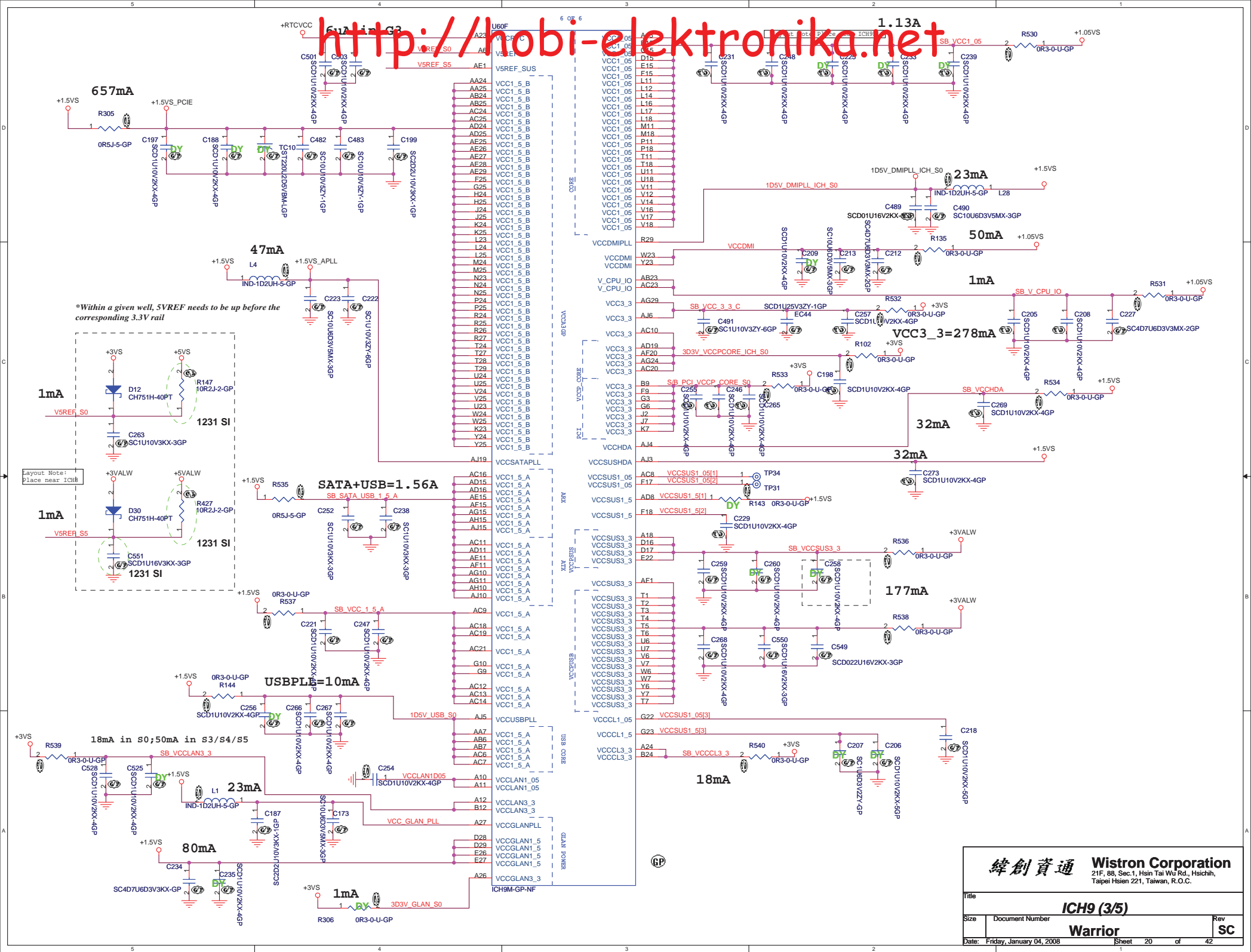
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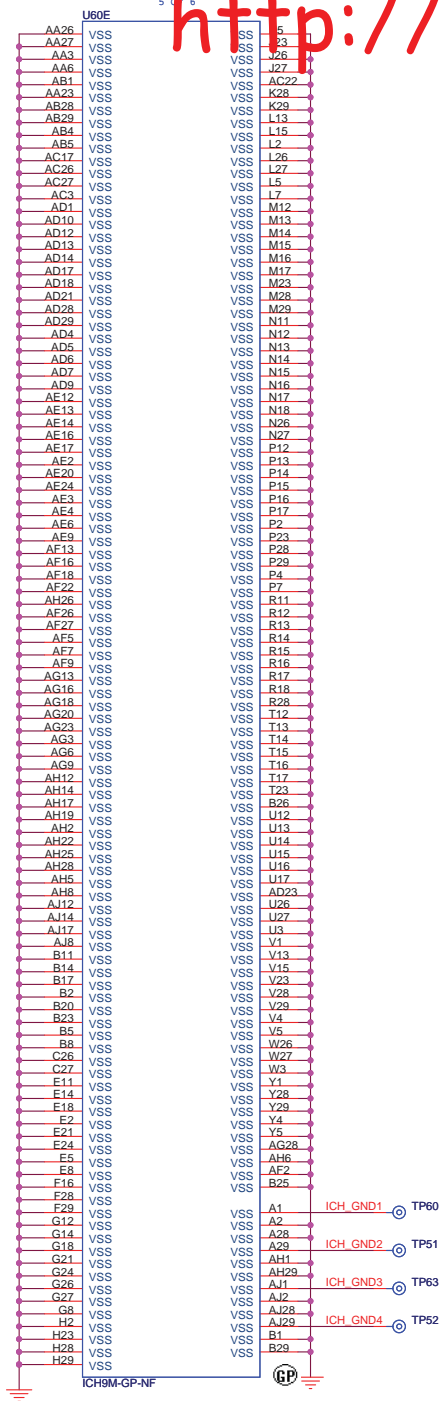
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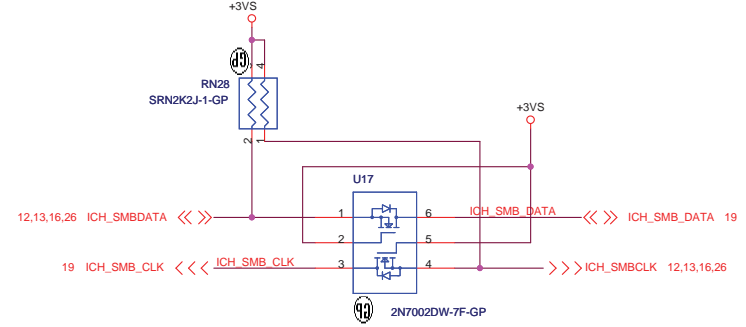


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ICH_GND1 TP60
ICH_GND2 TP51
ICH_GND3 TP63
ICH_GND4 TP52

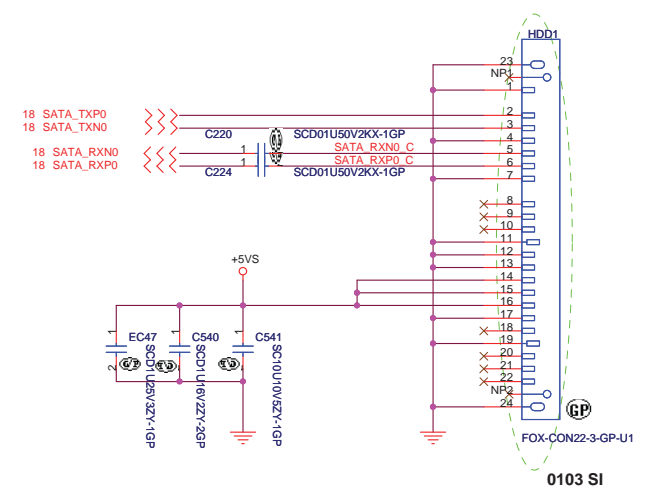
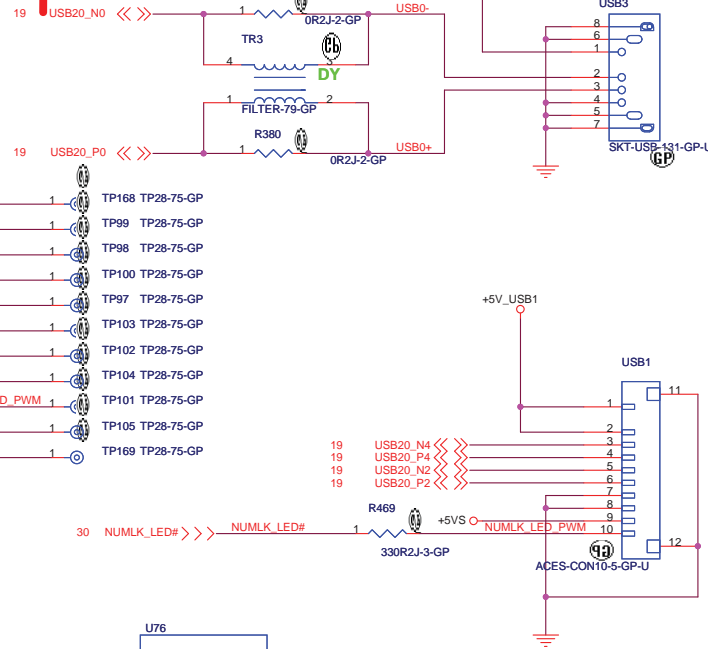
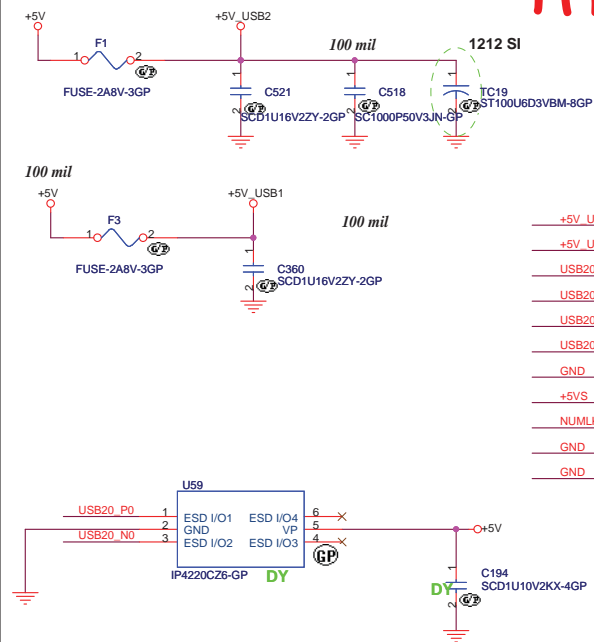
NCTF PIN



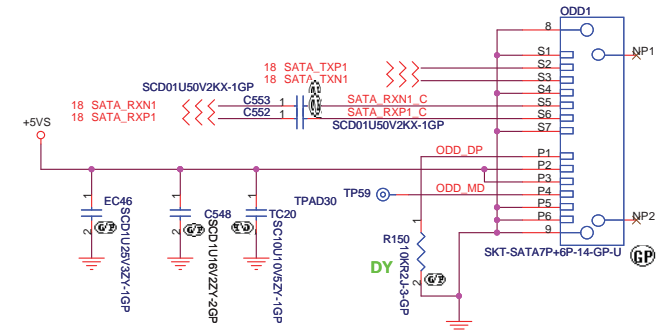
SMBUS

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Title ICH9-M (4 of 4)	
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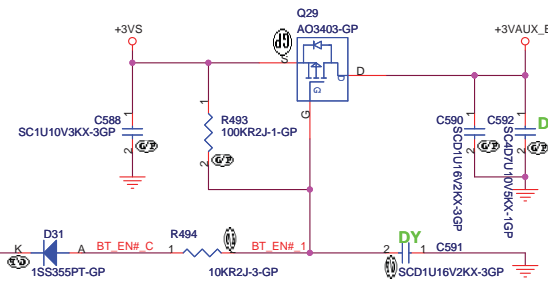
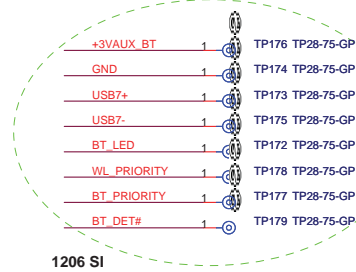
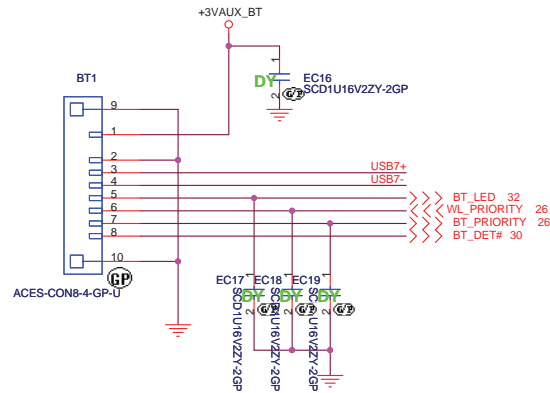
USB PORT



ODD Connector

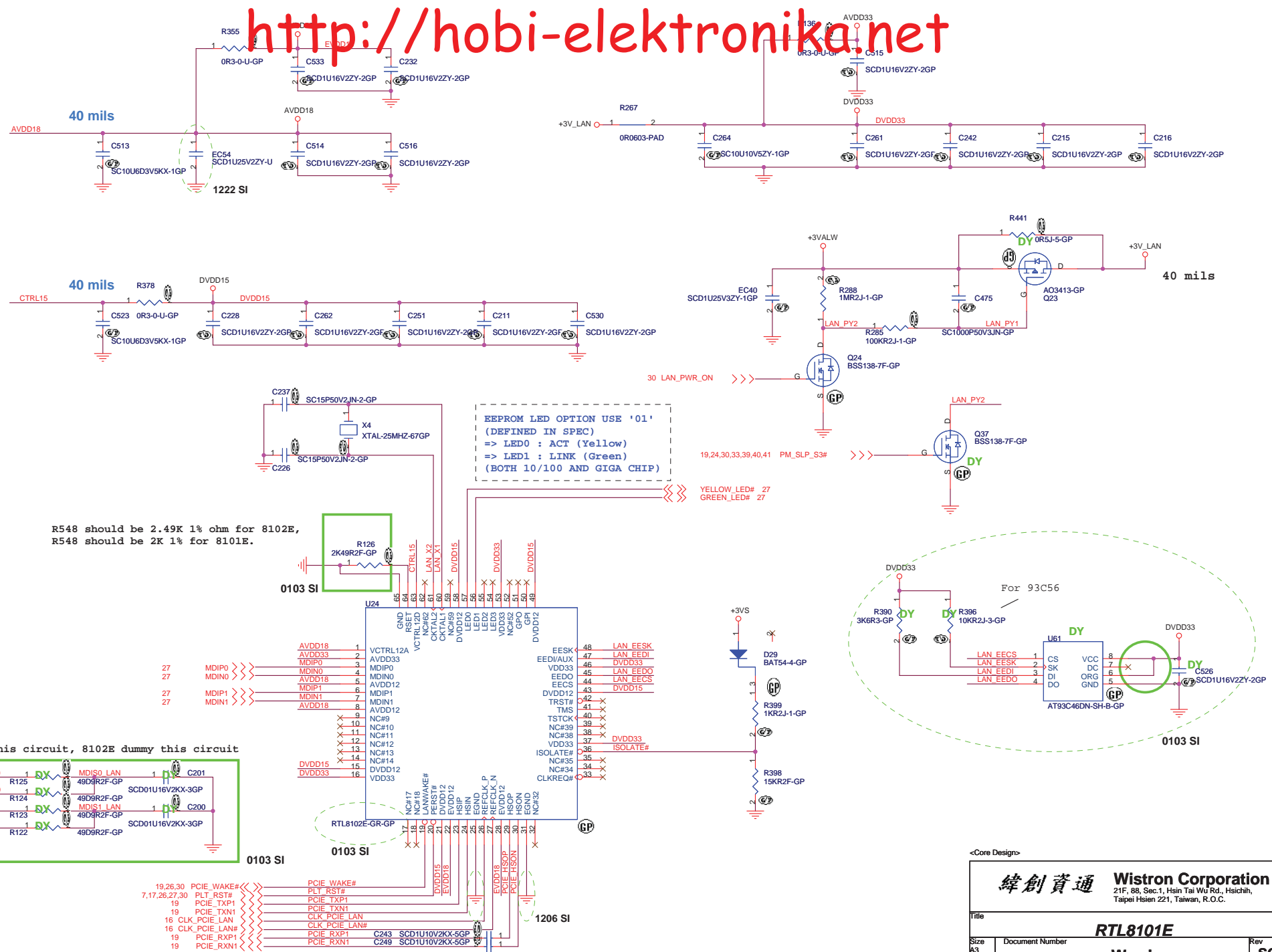


BLUETOOTH



<Core Design>

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HDD/CDROM/USB/BT	
Title Size A3 Date: Monday, January 07, 2008	Document Number Warrior Sheet 22 of 42
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Title			
<i>Thermal/Fan Controllor</i>			
Size	Document Number	Rev	
Custom	Warrior	SC	
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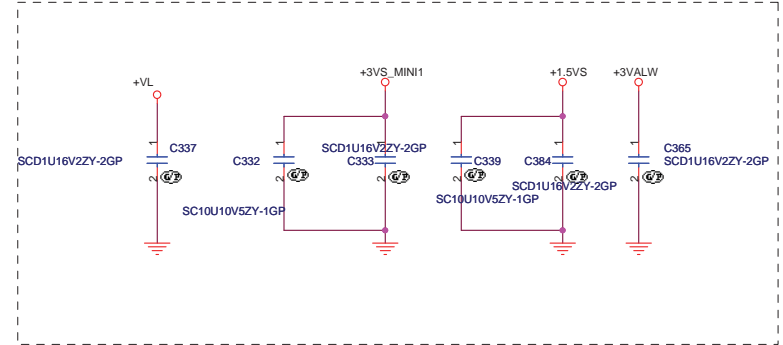
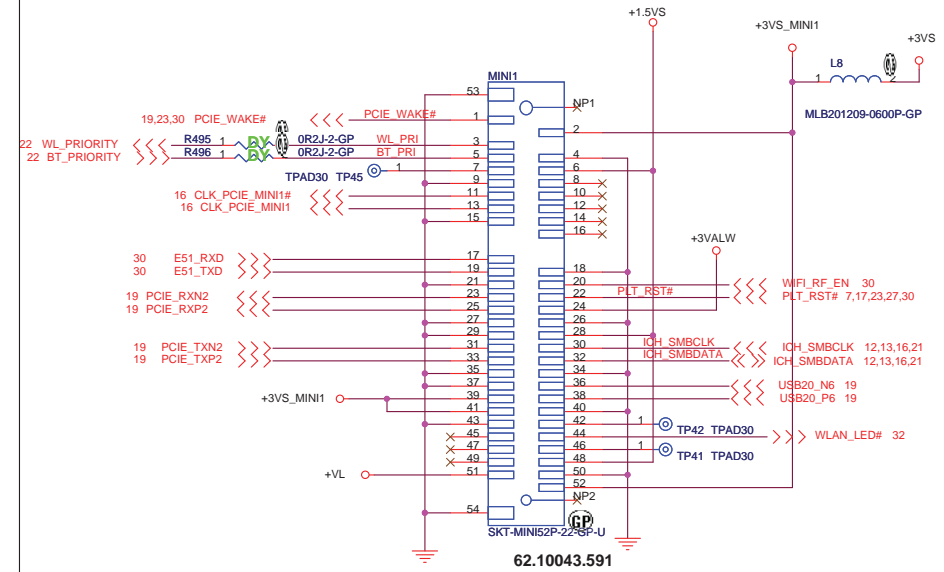
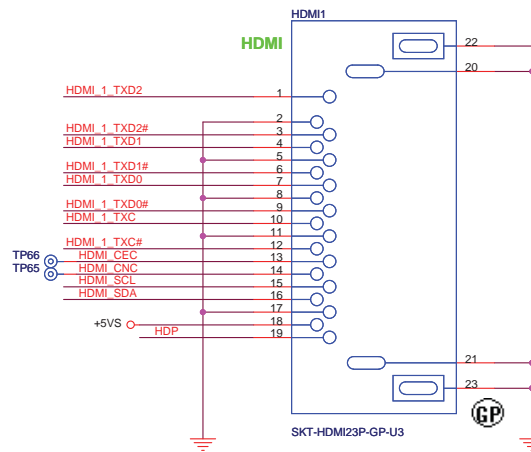
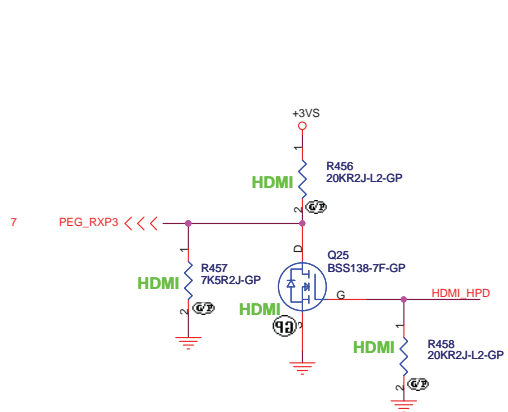
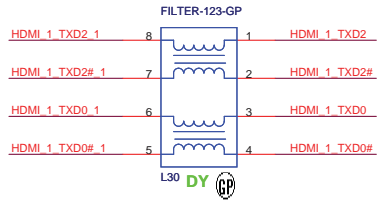
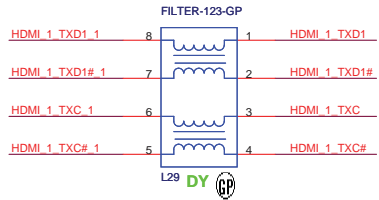
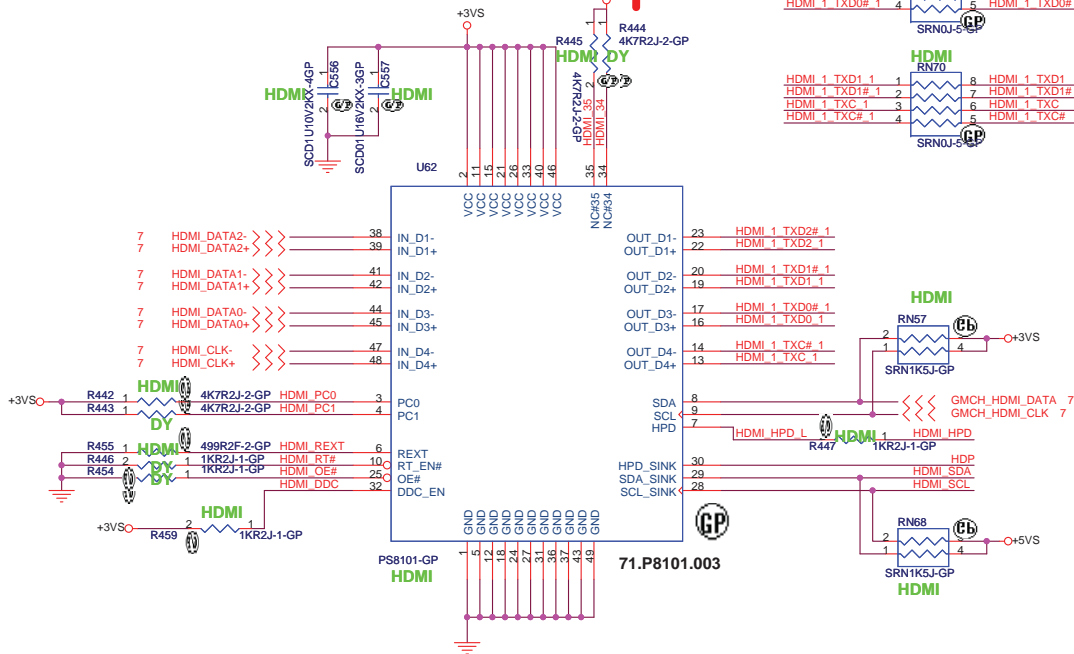
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
USB Card Reader Controller - RTS5158

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HDMI Connector

<http://hobi-elektronika.net>



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Title

Size

Document Number

MINI CARD/HDMI CONN .

Warrior

Rev

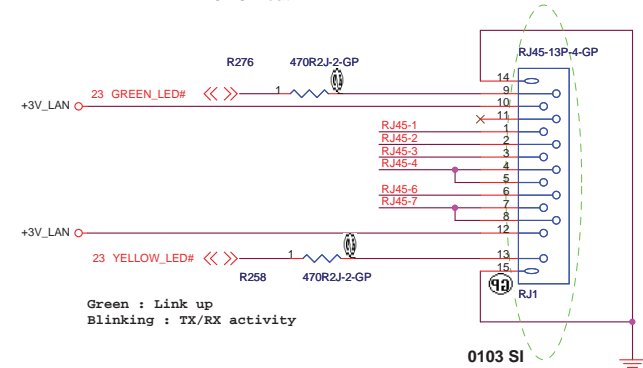
Date: Monday, January 07, 2008

Sheet

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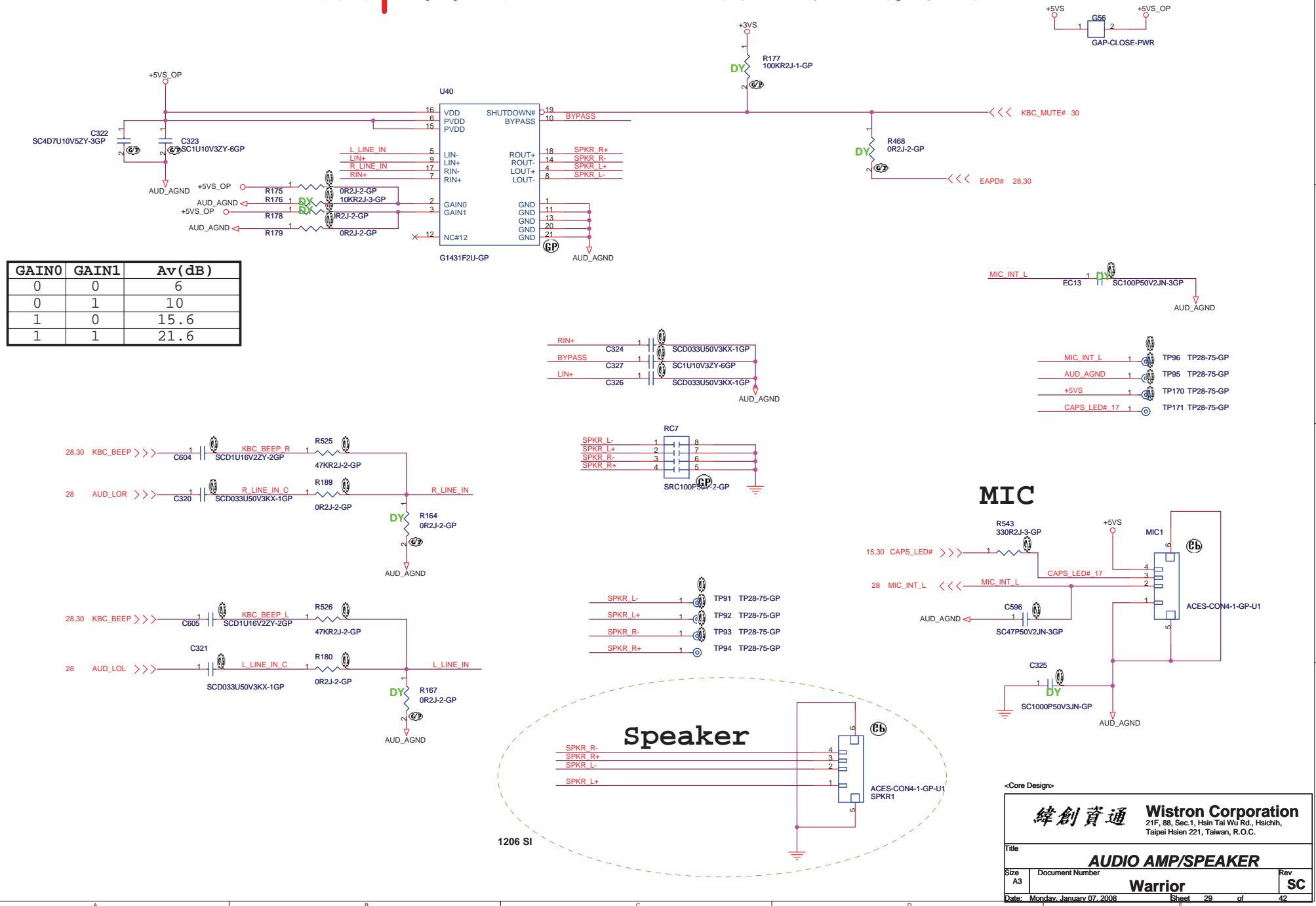
42

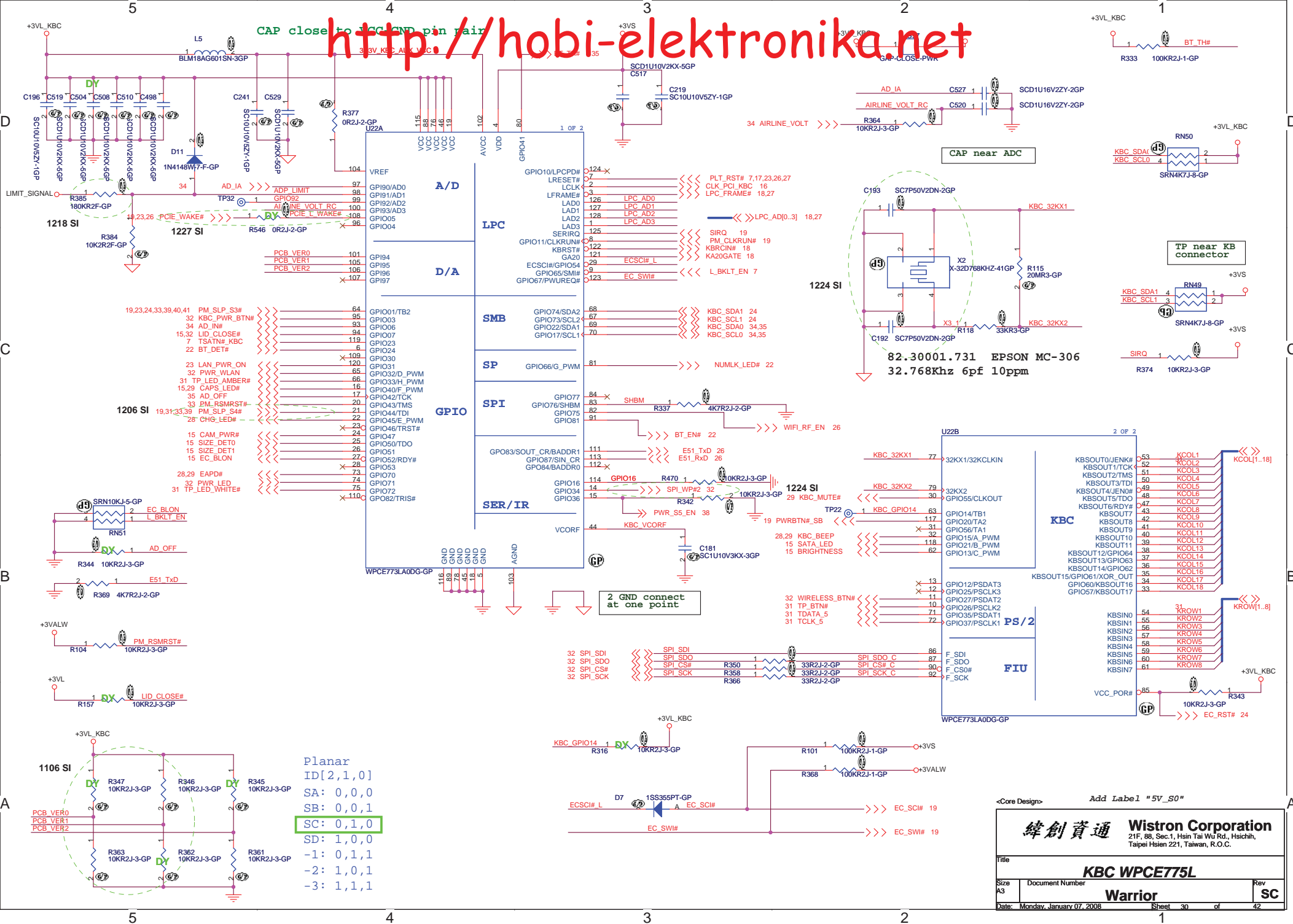
PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



```
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.
```

Golden Finger for Debug Board



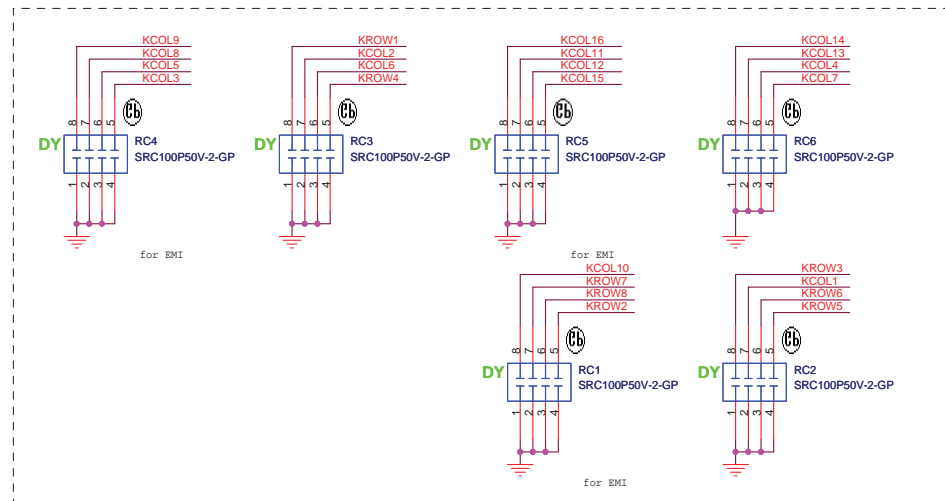
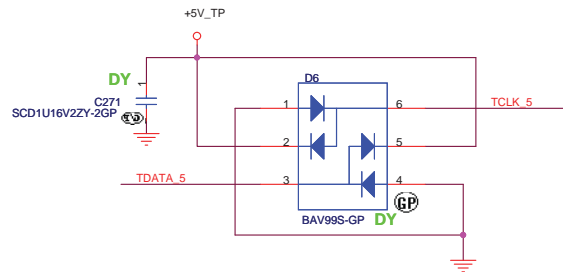
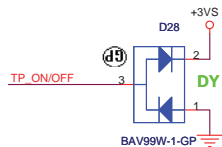


Internal KeyBoard Connector

30 KROW[1..8] <<< <<< <<<
30 KCOL[1..18] <<< <<< <<<

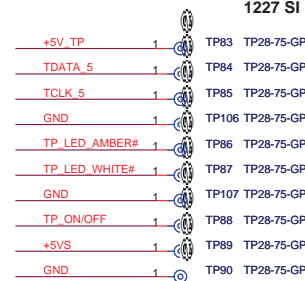
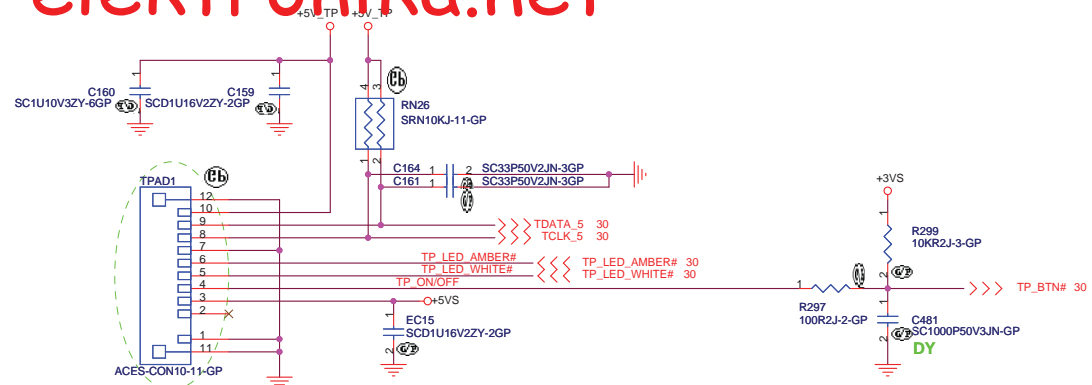
Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

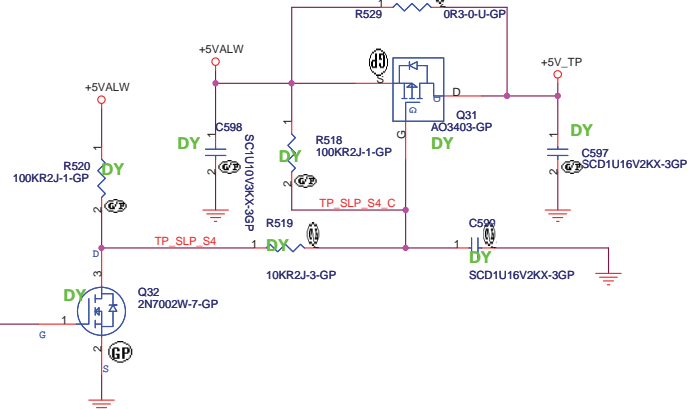


http://hobi-elektronika.net

TouchPad Connector



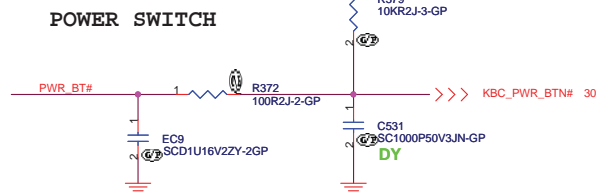
Please populate close TPAD1

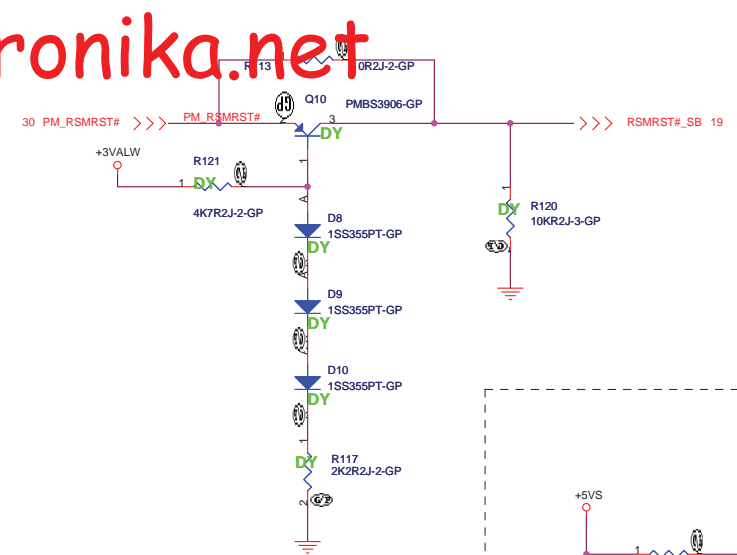
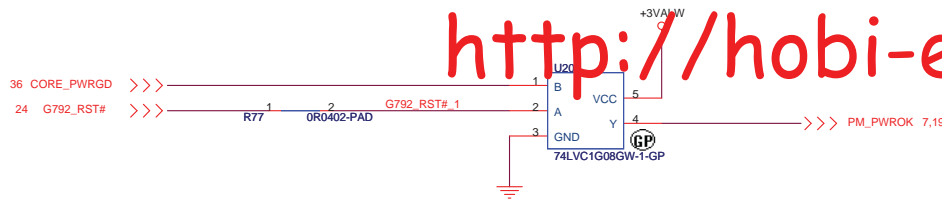


<Core Design>

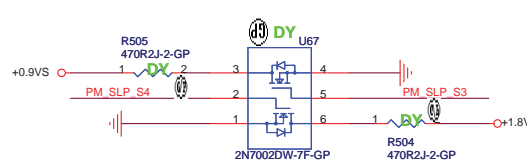
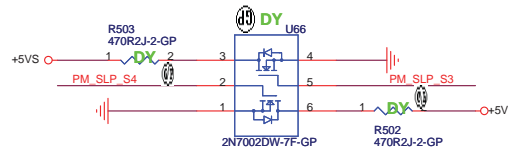
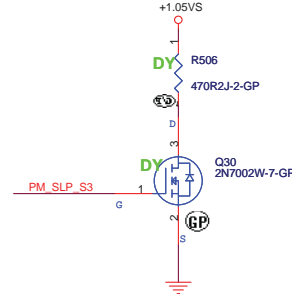
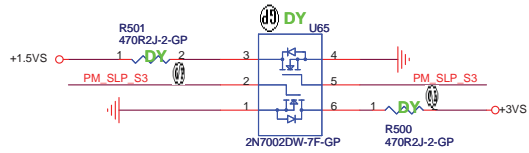
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Title			
KeyBoard-CONN			
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Discharge Circuit

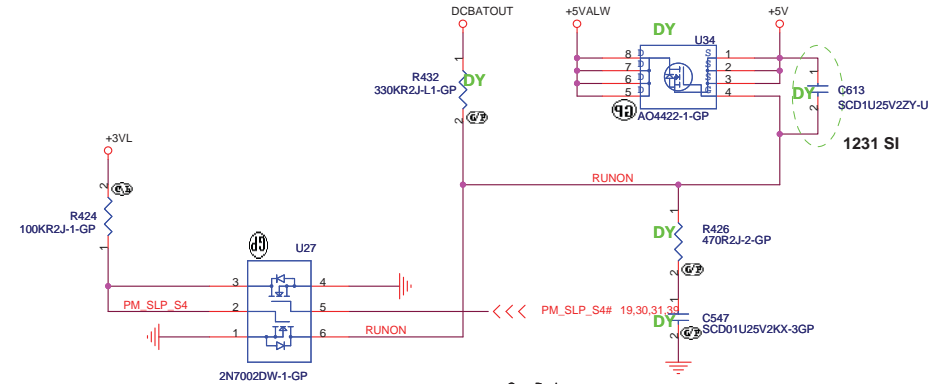
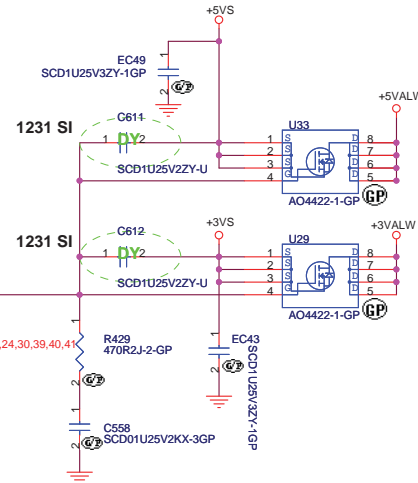
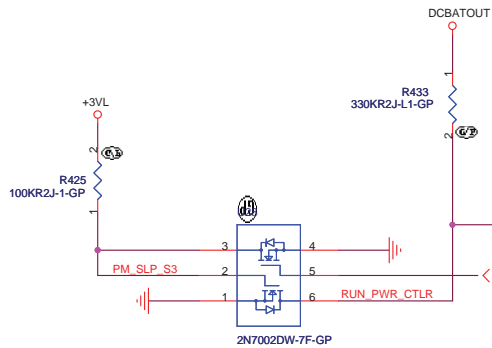


Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

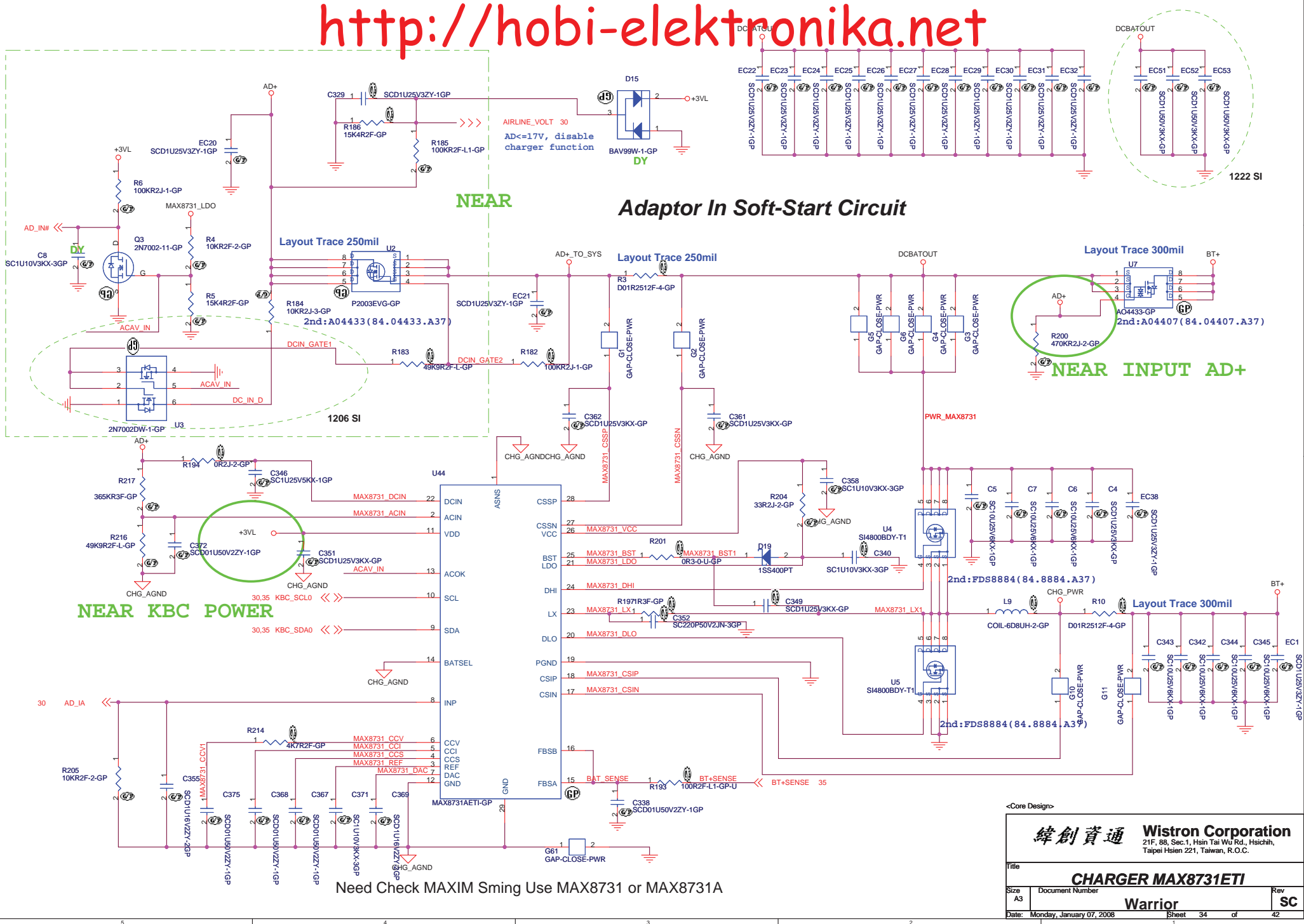
+5VALW to +5V Transfer

Run Power



<Core Design>

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BATTERY CONNECTOR



&ltCore Design>

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Title

AD/BATT CONN

Size

Document Number

Warrior

Rev

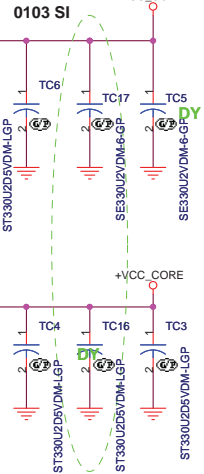
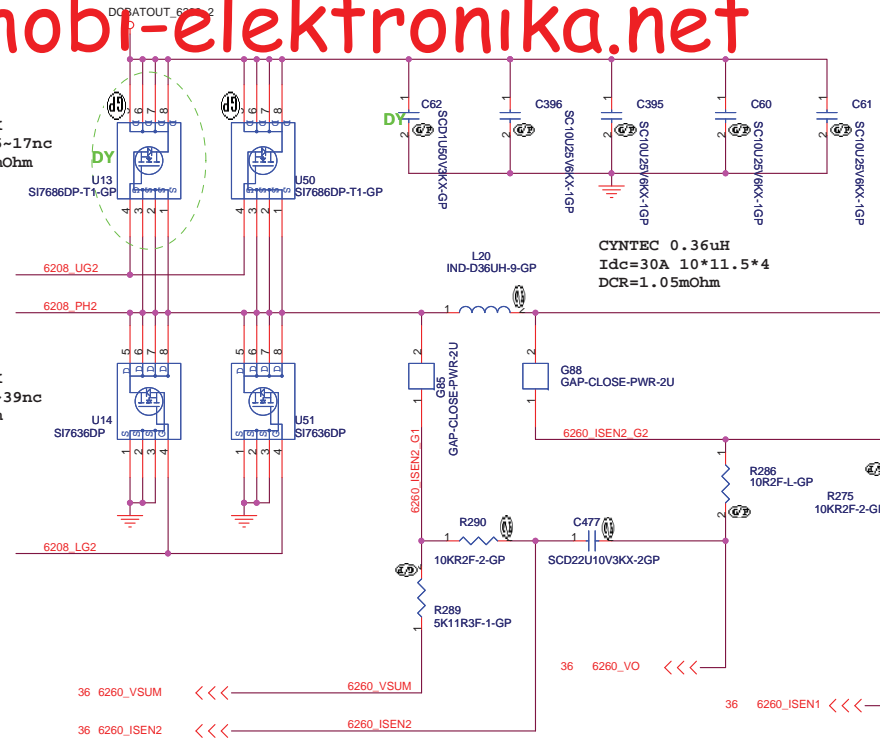
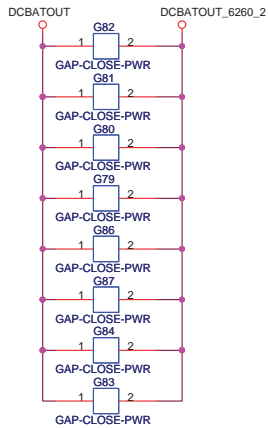
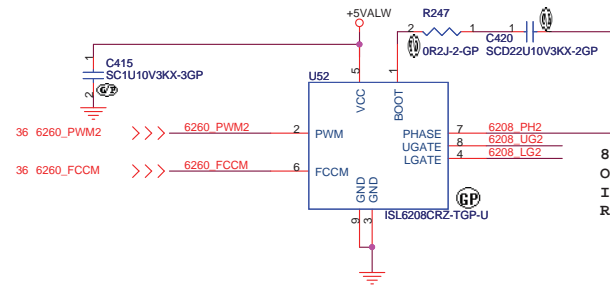
SC

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84.04841.037
ON4841 POWERPAK
Id=57A, Qg=11.5~17nc
Rdson=9.2~11.4mOhm

84.04835.F37
ON4835 POWERPAK
Id=104A, Qg=22~39nc
Rdson=4.3~5mOhm

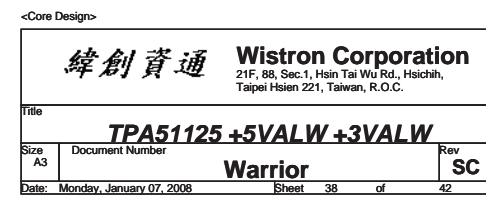


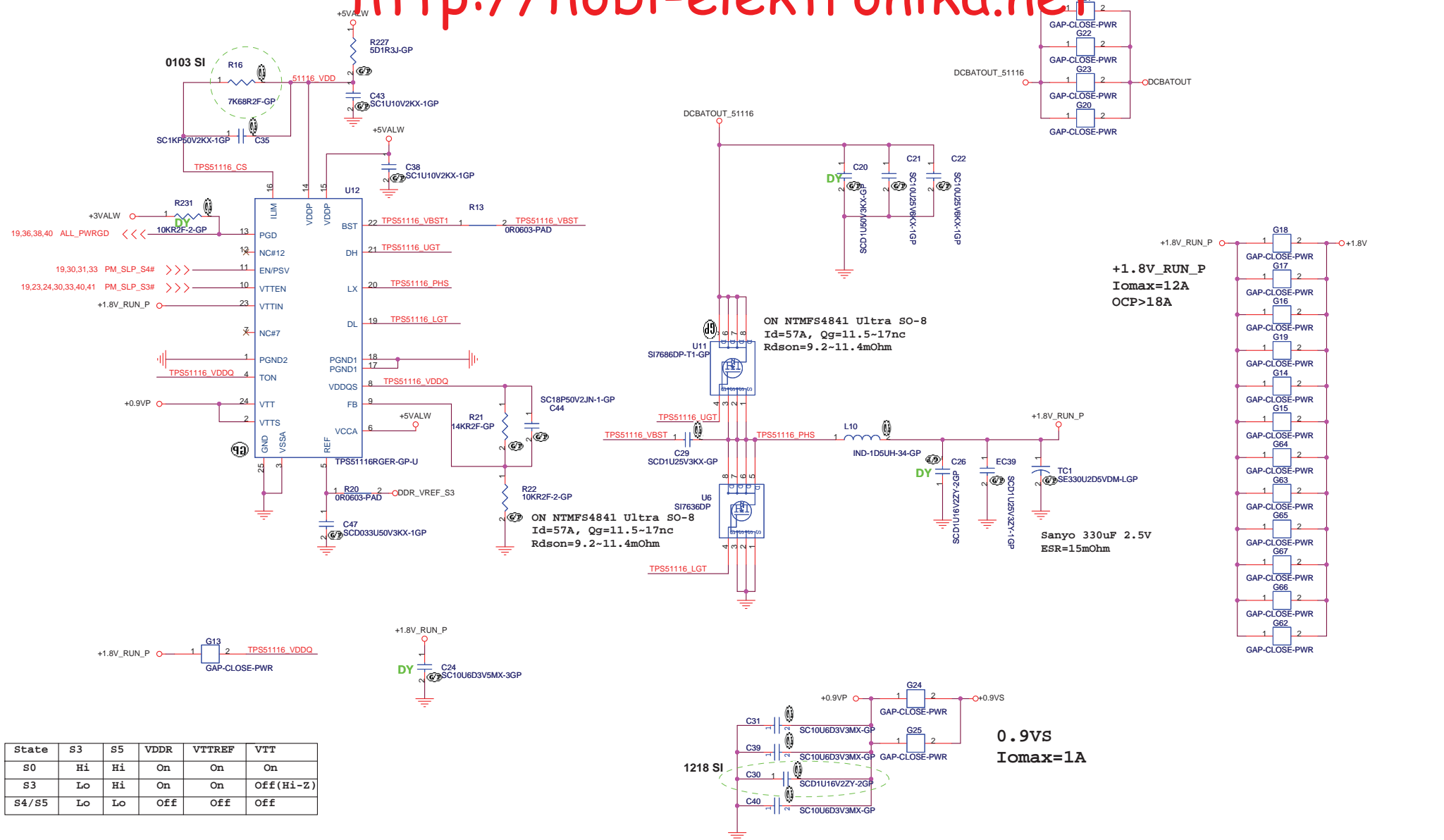
Kemet 330uF, 2.5V
ESR=9mΩ, Iripple=3.7A

<Core Design>

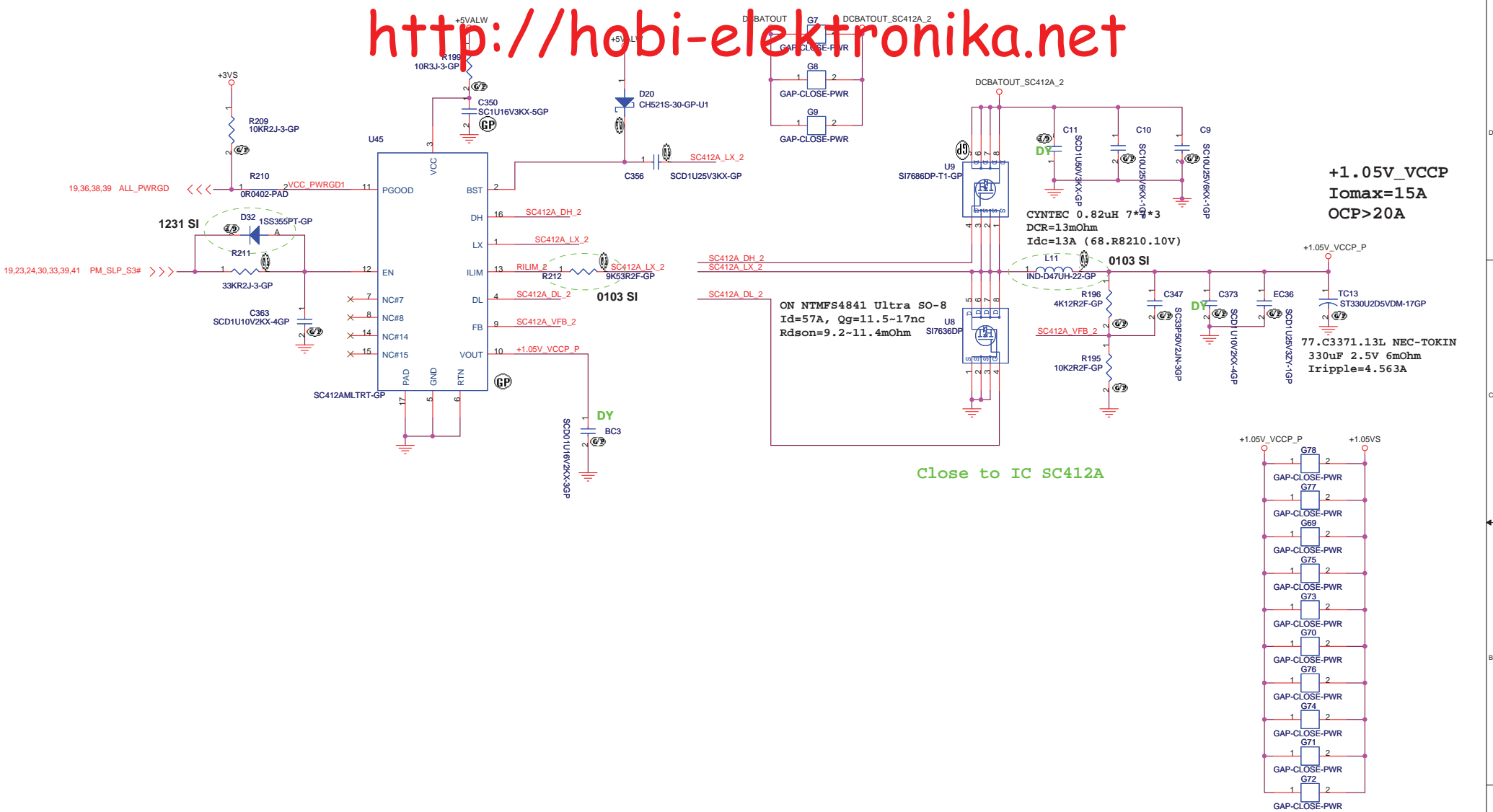
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			ISL6260CCRZ CPU CORE(2/2)	
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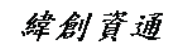
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



Close to IC SC412A

<Core Design>

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Title		
SC412A +1.05VS		
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Taipei Hsien 221, Taiwan, R.O.C.

Title

GMT 1D5V LDO

Size
A3

Document Number	
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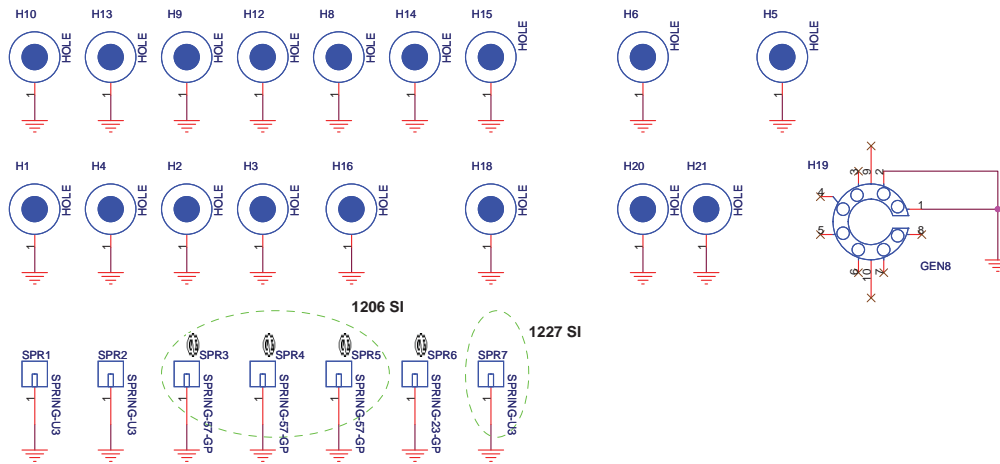
Warrior

SC

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2



SPR1-2: 34.40U07.001
SPR3-5: 34.42T14.002
SPR6 : 34.39S07.003
SPR7 : 34.40U07.001

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		MISC	
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